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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,247	07/18/2003	Sheldon C. P. Lim	CS01-150	3131
30402	7590	08/02/2005	EXAMINER	
WILLIAM STOFFEL			KIM, PAUL L	
PMB 455			ART UNIT	
1735 MARKET ST. - STE. A			PAPER NUMBER	
PHILADELPHIA, PA 19103-7502			2857	

DATE MAILED: 08/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/622,247	Applicant(s) LIM, SHELDON C. P. 	
	Examiner Paul Kim	Art Unit 2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 May 2005.  
 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) ☒ Claim(s) 7-20 is/are allowed.  
 6) ☒ Claim(s) 1-6 and 21-26 is/are rejected.  
 7) ☒ Claim(s) 27 is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☐ All    b) ☐ Some \*    c) ☐ None of:  
         1. ☐ Certified copies of the priority documents have been received.  
         2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
     \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Election/Restrictions***

1. Reply to restriction requirement filed on April 21, 2005 has been successfully traversed. All claims have been examined.

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsushita.

With regard to claims 1, 5, and 6, Matsushita teaches a test method comprising: obtaining test measurement values on a device at a plurality of independent variable values (col. 2, lines 10-22), calculating goodness of fit value for a fitted curve between a resistance and independent value (fig. 2), and using the goodness of fit to monitor the process (col. 1, lines 28-33).

With regard to claim 4, Matsushita teaches the goodness of fit being a standard error measurement (col. 1, lines 60-62).

4. Claims 25 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kashino et al.

With regard to claim 25, Kashino et al teaches providing a device structure that has a first test structure in which a test measurement can be obtained (col. 2, lines 1), measuring a first test measurement (col. 5, lines 20), calculating a goodness of fit value for a fitted curve between a first and second test measurement under a first and second test condition (fig. 2), and using the goodness of fit value to control the processes used to form the test structure (col. 2, lines 39-42).

With regard to claim 26, Kashino et al teaches the first and second test conditions being different temperatures (fig. 1, step S2).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Littau et al.

Matsushita teaches goodness of fit being calculated does not specify control limits being used. Littau et al teaches control limits being used for determining goodness of fit parameters (§ 107). It would have been obvious to one of ordinary skill in the art at the time of the invention, to modify Matsushita, so that control limits are used, as taught by Littau et al, in order to improve legitimacy of calculated values.

7. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kashino et al in view of Park et al.

Kashino et al teaches a method comprising: fabricating multiple test structures on a wafer incorporating a resistive structure (col. 2, lines 1+), measuring the resistance and deriving the sheet resistance from the resistance measurement (col. 5, lines 20+), calculating the goodness of fit value between one divided by the sheet resistance and a temperature (fig. 2), and using the goodness of fit value to control the processes used to form the test structure (col. 2, lines 39-42). Kashino et al, however, does not specify the resistive portion having an effective length and width, the effective length being substantially greater than the effective width. Park et al teaches a method for calculating goodness of fit of a wafer in which the effective length is substantially greater than the effective width (page 4, table 1). It would have been obvious to one of ordinary skill in the art at the time of the invention, to modify Kashino et al, so that the effective length is greater than the effective width, as taught by Park et al, in order to effectively monitor and control the fabrication process.

8. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita in view of Park et al.

Matsushita teaches a test method comprising: providing a device structure for which a test parameter is measured (col. 2, lines 10-22), measuring the test values on the structure, calculating a good of fit value for a fitted curve between the resistance and dimensional measurement (fig. 2), and using the goodness of fit to control the process

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(col. 1, lines 28-33). Matsushita, however, does not specify three test structures being measured. Park et al teaches a method for calculating goodness of fit of a wafer where at least three structures are measured (page 4, table 1). It would have been obvious to one of ordinary skill in the art at the time of the invention, to modify Matsushita, so that several structures are tested, as taught by Park et al, so as to derive the benefit of improved testing by thoroughly testing the wafer device.

### ***Allowable Subject Matter***

9. Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 7-20 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach a method for controlling the processing of semiconductor device in which goodness of fit is calculated by dividing the effective length by measured resistance.

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Harada teaches a sheet resistance meter for a wafer. Look et al

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teaches a resistor array for mask alignment detection. Baert et al teaches a method for analyzing stress in a polycrystalline layer.


12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Kim whose telephone number is 571-272-2217.

The examiner can normally be reached on Monday-Thursday 10:00-7:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300 for regular communications and for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

PK  
July 24, 2005

  
MARC S. HOFF  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800